Ch7 Structured Programming Quiz ANS

1. How many ones are in this 32-bit value 0xAAAAAAAA?

A) 8

B) 32

C) 16

D) 24

ANS: C. 16 (bits at odd positions 31, 29, 27, ..., 1 are all 1)

2. What does the instruction MOVS r0, r0, LSL #2 do?

A) To multiply r0 by 4

B) To shift left by 2 bits and update the Carry flag

C) To divide r0 by 4

D) To clear the register

ANS: B

3. In this instruction LDR r5, [r4, r2, LSL #2], what is the memory address that r5 is loaded from?

A) r4 + r2

B) r4 + (r2 × 2)

C) r4 + (r2 × 4)

D) r4 - (r2 × 4)

ANS: C

4. Which ARM instruction is used to compare two register values and set the CPU's status flags accordingly?

A) CMP

B) AND

C) MOV

D) SUB

ANS: A

5. Which instruction performs returning from a subroutine?

A) BX lr
B) MOV lr, pc
C) LDR r0, [r1]
D) CMP r1, r2

ANS: A

6. What does the instruction TST r1, r2 do?

A) Bitwise AND and updates N and Z flags

B) Bitwise XOR and updates all flags

C) Bitwise OR and updates N and Z flags

D) Logical AND and sets all flags

ANS: A

7. What does the instruction ADR r1, label do?

A) Loads the address of label into r1

B) Adds the value at label to r1

C) Loads label into program counter

D) None of the above

ANS: A

8. What is the equivalent ARM instruction for the C statement a &= b;?

A) AND r0, r0, r1

B) ORR r0, r0, r1

C) EOR r0, r0, r1

D) SUB r0, r0, r1

ANS: A

9. What ARM condition code suffix is used for a branch if the Zero flag is set after a comparison?

A) NE

B) GT

C) EQ

D) AL

ANS: C

10. What does the ARM instruction TST r1, #1 check?

A) If the least significant bit of r1 is set

B) If the least significant bit of r1 is cleared

C) If the most significant bit of r1 is set

D) If the most significant bit of r1 is cleared

ANS: A