Ch6 ARM Control Flow Quiz ANS

Q1

Which condition flag is set to 1 when the result of an operation is zero?

A) N (Negative flag)

B) Z (Zero flag)

C) C (Carry flag)

D) V (Overflow flag)

Q1 ANS: B - The Z (Zero) flag is set to 1 when all bits of the result are 0.

Q2

For unsigned subtraction, when is the Carry flag (C) set to 0?

A) When no borrow occurs

B) When a borrow occurs

C) When the result is negative

D) When overflow occurs

Q2 ANS; B - For unsigned subtraction, C = 0 (borrow = 1) when borrow takes place, meaning the true result < 0.

Q3

The Overflow flag (V) is set to 1 when:

A) Adding two different-signed numbers

B) Adding two same-signed numbers produces opposite sign result

C) Performing any multiplication

D) Using MOV instruction

Q3 ANS: B - V = 1 when adding 2 same-signed numbers produces a result with the opposite sign (Positive + Positive = Negative, or Negative + Negative = Positive).

Q4

What does the CMP R1, R2 instruction do?

A) Saves the result of R1 - R2

B) Performs R1 - R2 and discards the result

C) Performs R1 + R2 and sets flags

D) Moves R2 to R1

Q4 ANS: B - CMP performs subtraction R1 - R2, same as SUBS, except the result is discarded (not written to destination register).

Q5

The TST instruction performs which operation?

A) R1 + R2

B) R1 - R2

C) R1 & R2 (bitwise AND)

D) R1 ^ R2 (bitwise XOR)

Q5 ANS: C - TST performs bitwise AND on R1 and R2, same as ANDS, except the result is discarded.

Q6

When using TEQ instruction, the Z flag is set to 1 when:

A) R1 is greater than R2
B) R1 and R2 are equal
C) R1 is less than R2
D) An overflow occurs

Q6 ANS: B - TEQ performs XOR operation. If R1 and R2 are equal, then R1 ⊕ R2 is zero, and Z is set to 1.

Q7

Which instruction branches to a label and saves the return address in the link register (r14)?

A) B label
B) BX Rm
C) BL label
D) BLX Rm

Q7 ANS: C - BL (Branch with Link) copies the address of the next instruction into r14 (link register) and branches to the label.

Q8

For signed comparison, which branch instruction is used for 'greater than'?

A) BHI
B) BGT
C) BHS
D) BLO

Q8 ANS: B - BGT (Branch if signed Greater Than) is used for signed comparison, while BHI is for unsigned comparison.

Q9

The BGE (Branch if signed Greater or Equal) instruction tests which condition?

A) N = 1
B) Z = 1
C) N = V
D) C = 1

Q9 ANS: C - BGE tests the condition N = V, which indicates signed greater than or equal.

Q10

Which values represent 0xFFFFFFFF and 0x00000001 when interpreted as unsigned numbers?

A) -1 and 1
B) 2^32 - 1 and 1
C) 1 and -1
D) 255 and 1

Q10 ANS: B - When interpreted as unsigned 32-bit numbers, 2^32 – 1 = 4294967295 and 0x00000001 = 1.

Q11

In the instruction 'ADDLT r3, r2, r1', when is the ADD operation executed?

A) When N = V
B) When N != V
C) When Z = 1
D) When C = 1

Q11 ANS: B - ADDLT (Add if signed Less Than) executes when N != V, indicating a signed less than condition.

Q12

In a for loop implementation using 'SUBS r1, r1, #1' followed by 'BNE loop', what does this accomplish?

A) Increments counter and loops if zero
B) Decrements counter and loops if not zero
C) Sets flags without changing register
D) Unconditional branch

Q12 ANS: B - SUBS decrements the counter and sets flags, BNE branches back to loop if the result is not zero (Z=0).

Q13

The CBZ instruction is equivalent to which sequence?

A) CMP R1, #0; BNE label
B) CMP R1, #0; BEQ label
C) ADD R1, #0; BEQ label
D) SUB R1, #0; BNE label

Q13 ANS: B - CBZ R1, label is equivalent to CMP R1, #0 followed by BEQ label, except CBZ doesn't change status flags.

Q14

For signed comparison after 'CMP r0, r1', if N=0 and V=0, what can be concluded?

A) r0 < r1
B) r0 >= r1
C) r0 = r1
D) Overflow occurred

Q14 ANS: B - When N=0 and V=0, there's no overflow and the result is non-negative, so r0 - r1 >= 0, meaning r0 >= r1

Q15

In ARM Thumb-2, what does 'ITE' stand for in IT blocks?

A) If-Then-Else with 2 instructions
B) If-Then-End
C) Iterate-Then-Exit
D) If-Test-Execute

Q15 ANS: A - ITE stands for If-Then-Else, allowing 2 following instructions where the first executes if condition is true, second if false.

Q16

Which condition code tests for 'unsigned higher'?

A) HS
B) HI
C) GT
D) GE

Q16 ANS: B - HI (unsigned HIgher) tests C=1 & Z=0, while HS tests C=1 (unsigned Higher or Same).

Q17
In the assembly sequence ‘TEQ r0, #’!‘; TEQNE r0, #’?’’, what programming concept is being implemented?

A) Logical AND
B) Logical OR with short-circuit evaluation
C) Nested if statements
D) Switch statement

Q17 ANS: B - This implements logical OR (||) with short-circuit evaluation. The second TEQ only executes if the first test failed (NE condition).

Q18
The BLS (Branch if unsigned Lower or Same) instruction tests which condition?

A) C=0 or Z=1
B) C=1 and Z=0
C) N=V
D) N!=V

Q18 ANS: A - BLS tests C=0 or Z=1, meaning either the carry is clear (indicating lower) or zero flag is set (indicating same).

Q19
Which method is used to update condition flags with arithmetic operations?

A) Always automatic
B) Append ‘S’ to instruction or use compare instructions
C) Use special flag register
D) Only with branch instructions

Q19 ANS: B - Method 1: append ‘S’ (like ADDS) to update flags with result. Method 2: use compare instructions (CMP, CMN, TEQ, TST) that set flags only.

Q20
In break and continue statements, what is the key difference in assembly implementation?

A) Break uses BEQ, continue uses BNE
B) Break branches out of loop, continue branches to loop increment/test
C) Break sets flags, continue doesn’t
D) No difference in assembly

Q20 ANS: B - Break branches completely out of the loop (to end), while continue branches to the loop’s increment/condition test part to start the next iteration.

Quick Reference Summary

Key Condition Codes:

- **EQ/NE**: Z=1 / Z=0 (Equal/Not Equal)
- **LT/GE**: N≠V / N=V (Signed Less Than/Greater Equal)
- **GT/LE**: Z=0 & N=V / Z=1 or N≠V (Signed Greater/Less Equal)
- **LO/HS**: C=0 / C=1 (Unsigned Lower/Higher Same)
- **HI/LS**: C=1 & Z=0 / C=0 or Z=1 (Unsigned Higher/Lower Same)

Flag Setting Instructions:

- **CMP**: R1 - R2 (result discarded)
- **TST**: R1 & R2 (result discarded)
- **TEQ**: R1 ⊕ R2 (result discarded)

- **CMN**: R1 + R2 (result discarded)