Ch5 ARM Load Store Quiz ANS

1. In ARM memory, a word contains how many bits?
   A) 8
   B) 16
   C) 32
   D) 64

   ANS: C

2. For proper alignment, a 32-bit word must be stored at an address that is divisible by which value?
   A) 2
   B) 3
   C) 4
   D) 8

   ANS: C

3. In Little Endian format, where is the least significant byte of a word placed in memory?
   A) Highest address of the word
   B) Lowest address of the word
   C) Middle byte of the word
   D) Location is unspecified

   ANS: B

4. Which instruction loads a 32-bit word from memory into a register?
   A) STR
   B) LDR
   C) LDRB
   D) STRH

   ANS: B

5. Which instruction loads an unsigned byte and zero-extends it to 32 bits?
   A) LDRSB
   B) LDRH
   C) LDRB
   D) LDRSH

   ANS: C

6. The difference between LDRH and LDRSH is that LDRH zero-extends the halfword, while LDRSH does what?
   A) Sign-extends the halfword

B) Truncates to 8 bits
C) Reverses byte order
D) Doubles the value

ANS: A

7. In pre-index addressing LDR r1, [r0, #4], what happens to r0 after the load?
   A) r0 is incremented by 4 before the load
   B) r0 is incremented by 4 after the load
   C) r0 remains unchanged
   D) r0 is decremented by 4

   ANS: C

8. What does the exclamation mark indicate in LDR r1, [r0, #4]! ?
   A) Post-index addressing
   B) Pre-index with update
   C) Syntax error
   D) PC-relative addressing

   ANS: B

9. In post-index addressing LDR r1, [r0], #4, when is r0 updated?
   A) Before the memory access
   B) After the memory access
   C) During the memory access
   D) It is never updated

   ANS: B

10. Assume Little Endian and r0 = 0x20008000 with memory contents: [0x20008000]=0xEF, [0x20008001]=0xCD, [0x20008002]=0xAB, [0x20008003]=0x89; what does LDRH r1, [r0] load into r1?
    A) 0x0000EFCD
    B) 0x0000CDEF
    C) 0x89ABCDEF
    D) 0x000089AB

    ANS: B (Load halfword and zero-extension)

11. What happens when you execute LDRSB r1, [r0] and the byte at the memory location has value 0xEF?
    A) r1 = 0x000000EF
    B) r1 = 0xFFFFFFEF
    C) r1 = 0xEF000000
    D) r1 = 0x0000FFEF

ANS: B (LDRSB sign-extends, 0xEF is negative so extends with 1s)

12. Which store instruction writes only the low 16 bits of a register to memory?
    A) STR
    B) STRB
    C) STRH
    D) STRSH

    ANS: C

13. In LDR r1, [r0, r2, LSL #2], what is the effective address used?
    A) r0 + r2
    B) r0 + (r2 × 2)
    C) r0 + (r2 × 4)
    D) r0 + (r2 × 8)

    ANS: C

14. Which statement about register order in LDM/STM is correct?
    A) Stored/loaded in the order listed
    B) Lowest-numbered register uses the lowest address
    C) Highest-numbered register uses the lowest address
    D) Order is undefined

    ANS: B

15. Which mnemonic expansion is correct for STMDB?
    A) Store Multiple Decrement Before
    B) Store Multiple Decrement After
    C) Store Transfer Memory Decrement Before
    D) Store Transfer Multiple Decrement After

    ANS: A

16. In post-index addressing LDR r1, [r0], #4, when is r0 updated?
    A) Before the memory access
    B) After the memory access
    C) During the memory access
    D) r0 is never updated

    ANS: B

17. In the instruction LDR r1, [r0, r2], what does r2 represent?
    A) The destination register
    B) The base register
    C) The offset register
    D) An immediate value

ANS: C

18. What happens if an LDR pseudo-instruction's constant cannot be encoded with MOV/MVN/MOVW?
    A) The assembler errors out
    B) It becomes a STR to literal pool
    C) A PC-relative LDR from a literal pool is generated
    D) It becomes an ADR instruction

    ANS: C

19. ADR is a pseudo-instruction that primarily does which of the following?
    A) Loads an absolute 32-bit address directly
    B) Loads a program-relative address into a register
    C) Stores a register into memory
    D) Performs an arithmetic add on two registers

    ANS: B

20. On Cortex-M, what is the default endianness and configurability mentioned in the slides?
    A) Big Endian only, fixed
    B) Little Endian by default, can be configured to Big Endian
    C) Mixed Endian, configurable
    D) Big Endian by default, can be configured to Little Endian

    ANS: B