Ch4 ARM Arithmetic Logic Quiz

1. What is the effect of appending the suffix S to most ARM data-processing instructions?
   A. It updates the N, Z, C, V flags in the APSR register.
   B. It enables conditional execution for the instruction.
   C. It forces the instruction to use Thumb encoding only.
   D. It swaps the operands before execution.

   ANS:

2. Which of the following is the Unified Assembler Language (UAL) syntax for adding two registers r2 and r3 and placing the result in r1?
   A. ADD r1, r3
   B. ADD r1, r2, r3
   C. ADD r1, #15
   D. ADD r2, r1, r3

   ANS:

3. What does ADC do in ARM assembly?
   A. Rd ← Rn − Op2 − 1
   B. Rd ← Rn + Op2 + Carry
   C. Rd ← Op2 − Rn
   D. Rd ← Rn × Op2 + Ra

   ANS:

4. When adding two 64-bit integers split across two registers each, which instruction pair correctly handles the low and high halves?
   A. ADC for high halves, then ADDS for low halves to set carry
   B. ADC for low halves, then ADDS for high halves
   C. ADDS for low halves to set carry, then ADC for high halves
   D. ADD for low halves, then ADD for high halves

   ANS:

5. In ARM subtraction, what does the carry flag C indicate when a borrow occurs in SUBS?
   A. C = 1 when there is a borrow
   B. C = 0 when there is a borrow
   C. C toggles regardless of borrow
   D. C is always preserved from the previous instruction

   ANS:

6. Which instruction performs reverse subtraction in ARM?
   A. SBC

B. RSB
C. SUB
D. ADC

ANS:

7. Which instruction clears selected bits in Rd by ANDing Rn with NOT of Operand2?
   A. BFI
   B. BFC
   C. BIC
   D. MVN

   ANS:

8. The instruction BFC R4, #8, #12 has what effect?
   A. Inserts 12 bits from R4 into R8 starting at bit 12
   B. Clears bits 8 through 19 of R4
   C. Copies bits 8 through 19 of R4 into R12
   D. Sets bits 8 through 19 of R4 to ones

   ANS:

9. In C, what is the result of the expression 0x10 && 0x01?
   A. 0x00
   B. 0x10
   C. 0x01
   D. 0x11

   ANS:

10. Which instruction reverses the bit order within a 32-bit word?
    A. REV
    B. REV16
    C. REVSH
    D. RBIT

    ANS:

11. Which instruction reverses the byte order in each half-word independently?
    A. REV
    B. RBIT
    C. REV16
    D. REVSH

    ANS:

12. What is the effect of REVSH on a 32-bit register?
    A. Reverse all bits and zero-extend
    B. Reverse byte order in bottom half-word and sign extend to 32 bits
    C. Reverse byte order in each half-word without sign extension
    D. Reverse byte order in a word without sign extension

    ANS:

13. Which instruction zero-extends an 8-bit byte into a 32-bit register?
    A. SXTB
    B. UXTB
    C. SXTH
    D. UXTH

    ANS:

14. What is the correct sequence to load 0x87654321 into r0 using MOVW and MOVT?
    A. MOVT r0, #0x8765; MOVW r0, #0x4321
    B. MOVW r0, #0x4321; MOVT r0, #0x8765
    C. MOVW r0, #0x8765; MOVT r0, #0x4321
    D. MOVT r0, #0x4321; MOVW r0, #0x8765

    ANS:

15. Which of the following is not a barrel shifter operation in ARM?
    A. LSL
    B. ROR
    C. RRX
    D. ROL

    ANS:

16. How can a rotate-left by n bits be implemented on a 32-bit value using available rotate instructions?
    A. As RRX by n
    B. As ROR by 32 − n
    C. As LSL by 32 − n
    D. As ASR by n

    ANS:

17. Which shift corresponds to signed division by a power of two with sign extension?
    A. LSR
    B. ASR
    C. LSL
    D. ROR

ANS:

18. In the sequence ANDS r2, r1, r0, LSL #1, which flag value is affected by the preceding shift rather than the AND itself?
    A. N only
    B. Z only
    C. C only
    D. V only

    ANS:

19. Which pattern correctly toggles bit 5 of r0 without affecting other bits?
    A. ORRS r0, r0, r4, LSL #5 with r4 = 1
    B. ANDS r0, r0, r4, LSL #5 with r4 = 1
    C. EORS r0, r0, r4, LSL #5 with r4 = 1
    D. BICS r0, r0, r4, LSL #5 with r4 = 1

    ANS:

20. Which single instruction multiplies a register by 17 using the barrel shifter on the second operand?
    A. ADD r4, r4, r4, LSL #4
    B. RSB r5, r5, r5, LSL #5
    C. ADD r1, r0, r0, ASR #3
    D. MUL r1, r0, #17

    ANS: