Ch16 Timer PWM Quiz

Q1. What is the primary disadvantage of using Polling instead of Interrupts?
A. Polling is more complex to implement.
B. Polling wastes CPU cycles by continuously checking for events.
C. Polling cannot handle multiple devices.
D. Polling requires more hardware wiring than interrupts.
ANS:

2. In the ARM Cortex-M architecture, what is the role of the Nested Vectored Interrupt Controller (NVIC)?
A. To generate clock signals for the CPU.
B. To coordinate multiple interrupt sources, manage priorities, and enable/disable interrupts.
C. To automatically save all General Purpose Registers (R0-R15) to flash memory.
D. To convert analog signals to digital signals for processing.
ANS:

3. Where is the Interrupt Vector Table typically located in memory (before any relocation)?
A. 0x20000000
B. 0x08000000
C. 0x00000000
D. 0xFFFFFFFF
ANS: C

4. Which specific set of registers is automatically pushed onto the stack (Stacking) when an interrupt occurs?
A. R0–R12, SP, LR, PC
B. R0–R3, R12, LR, PC, xPSR
C. R4–R11, SP
D. All CPU registers (R0–R15)
ANS:

5. During the Stacking process, the Stack Pointer (SP) is:
A. Incremented by 32 bytes.
B. Decremented by 32 bytes (for a full descending stack).
C. Incremented by 4 bytes.
D. Left unchanged; registers are saved to a special buffer.
ANS:

6. What value does the Link Register (LR) hold when the processor is executing an Interrupt Service Routine (ISR)?
A. The address of the next instruction in the main program.
B. A special EXC_RETURN value (e.g., 0xFFFFFFF9) indicating how to return.
C. 0x00000000
D. The address of the ISR itself.
ANS:

7. Which Stack Pointer is selected by default at Reset?
A. Process Stack Pointer (PSP)
B. Main Stack Pointer (MSP)
C. Floating Point Stack Pointer
D. System Stack Pointer
ANS:

8. If SPSEL bit in the Control Register is 0, which stack pointer is used in Thread Mode?
A. MSP
B. PSP
C. Both MSP and PSP simultaneously
D. None of the above
ANS:

9. To exit an ISR and return to the main program, which instruction is typically used?
A. MOV PC, #0
B. BX LR
C. POP {R4-R11}
D. RET
ANS:

10. Which register is used to divide the CPU clock frequency to generate a slower Timer Clock frequency?
A. Auto-Reload Register (ARR)
B. Capture Compare Register (CCR)
C. Prescaler Register (PSC)
D. Control Register (CR1)
ANS:

11. If the CPU Clock is 16 MHz and PSC is set to 15999, what is the Timer Clock frequency (fCK_CNT)?
A. 16 MHz
B. 1 MHz
C. 1 kHz
D. 100 Hz
ANS:

12. In "Up-counting Mode," what happens when the Counter reaches the value in the Auto-Reload Register (ARR)?
A. It stops counting immediately.
B. It resets to 0 and generates an Update Event (UEV).
C. It reverses direction and starts counting down.
D. It waits for a software reset trigger.
ANS:

13. The formula for the Timer Period in Up-counting mode is:
A. (ARR + 1) * Clock Period
B. ARR * Clock Period
C. (PSC + 1) * ARR
D. 2 * ARR * Clock Period
ANS:

14. In "Center-aligned Counting Mode," the counter counts:
A. Up from 0 to ARR, then resets to 0.
B. Down from ARR to 0, then resets to ARR.
C. Up from 0 to ARR, then Down from ARR to 0.
D. Randomly between 0 and ARR.
ANS:

15. Which PWM Mode behaves as "Low True" (Active Low) in Up-counting mode?
A. PWM Mode 1
B. PWM Mode 2

C. Center-aligned Mode
D. Capture Mode
ANS:

16. In PWM Mode 1 (Up-counting), if CNT < CCR, the output is:
A. Active (High)
B. Inactive (Low)
C. Toggled
D. Undefined
ANS:

17. To increase the Duty Cycle in PWM Mode 1, you should:
A. Decrease the CCR value.
B. Increase the CCR value.
C. Set ARR to 0.
D. Increase the Prescaler (PSC).
ANS:

18. How is the Duty Cycle calculated for PWM Mode 1?
A. Duty Cycle = 1 - (CCR / (ARR + 1))
B. Duty Cycle = CCR / (ARR + 1)
C. Duty Cycle = (ARR + 1) / CCR
D. Duty Cycle = PSC / ARR
ANS:

19. A timer runs from a 72 MHz clock. PSC = 71 and ARR = 999. In PWM Mode 1, CCR = 250. What is the duty cycle?
A. 10%
B. 25%
C. 50%
D. 75%
ANS:

20. In center-aligned mode, a timer has ARR = 4000, PSC chosen so that the counter clock is 50 kHz. What is the PWM period?
A. 40 ms
B. 160 ms
C. 320 ms
D. 640 ms
ANS: